

WHAT IS CLAIMED IS:

1. An integrated circuit device, comprising
a semiconductor substrate;
a well region formed inside the semiconductor substrate;
a first isolation structure formed inside the well region;
5 a second isolation structure formed inside the well region and spaced apart
from the first isolation structure;
a dielectric layer disposed over the well region; and
a layer of silicon, formed over the dielectric layer, including a p-type portion,
an n-type portion and a center portion disposed between the p-type and n-type
10 portions, wherein the p-type portion overlaps the first isolation structure and the
n-type portion overlaps the second isolation structure.
2. The integrated circuit device as claimed in claim 1, wherein the center portion
of the layer of silicon is doped with an n-type impurity having a doped concentration
lower than that of the n-type portion.
3. The integrated circuit device as claimed in claim 1, wherein the center portion
of the layer of silicon is doped with a p-type impurity having a doped concentration
lower than that of the p-type portion.

4. The integrated circuit device as claimed in claim 1, wherein the center portion of the layer of silicon is undoped.
5. The integrated circuit device as claimed in claim 1, wherein the center portion overlaps a portion of the well region between the first and second isolation structures.
6. The integrated circuit device as claimed in claim 1, further comprising a diffused region formed inside the well region adjacent one of the first and second isolation structures.
7. The integrated circuit device as claimed in claim 6, wherein the diffused region is biased to cause the well region to be biased to control the silicon layer for providing electrostatic discharge protection.
8. An integrated circuit device receiving signals from a signal pad, comprising at least one substrate-biased silicon diode responsive to the signals from the signal pad for providing electrostatic discharge protection.
9. The integrated circuit device claimed in claim 8, wherein the at least one substrate-biased silicon diode includes one or more serially coupled substrate-biased silicon diodes.

10. The integrated circuit device as claimed in claim 8, wherein the at least one substrate-biased silicon diode includes a p-type polysilicon portion, an n-type polysilicon portion and a center polysilicon portion disposed between and contiguous with the p-type and n-type polysilicon portions.

11. The integrated circuit device as claimed in claim 10 further comprising,
a first isolation structure, and
a second isolation structure spaced apart from the first isolation structure,
wherein the p-type polysilicon portion overlaps the first isolation structure and
the n-type polysilicon portion overlaps the second isolation structure.

12. The integrated circuit device as claimed in claim 11, further comprising a diffused region inside a well region adjacent one of the first isolation structure and second isolation structure, wherein the diffused region is doped with a same impurity as the well region.

13. The integrated circuit device as claimed in claim 12, wherein the well region is biased to control the at least one substrate-biased silicon diode for providing electrostatic discharge protection.

14. The integrated circuit device as claimed in claim 12, wherein the diffused region is biased to cause the well region to be biased to control the at least one substrate-biased silicon diode for providing electrostatic discharge protection.
15. The integrated circuit device as claimed in claim 8, wherein the at least one substrate-biased silicon diode includes a p-portion and an n-portion, and wherein the signal pad is coupled to the p-portion of the at least one substrate-biased silicon diode.
16. The integrated circuit device as claimed in claim 8, further comprising a detection circuit for detecting the signals from the signal pad and providing a bias voltage to the at least one substrate-biased silicon diode.
17. The integrated circuit device as claimed in claim 8, wherein the signals from the signal pad are electrostatic pulses.
18. The integrated circuit device as claimed in claim 16, wherein the detection circuit comprises a resistor-capacitor circuit having a delay constant longer than the duration of the signals from the signal pad.
19. The integrated circuit device as claimed in claim 16, wherein the detection circuit comprises a resistor-capacitor circuit coupled in parallel to a transistor network.

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20. The integrated circuit device as claimed in claim 16, wherein the detection circuit includes a first transistor, a second transistor, and a resistor-capacitor circuit, and wherein a gate of the first transistor is coupled to a gate of the second transistor and the resistor-capacitor circuit.

21. The integrated circuit device as claimed in claim 20, wherein a drain of the first transistor and a drain of the second transistor are coupled to a substrate of the at least one substrate-biased silicon diode to provide a bias voltage.

22. The integrated circuit device as claimed in claim 20, wherein a source of the first transistor is coupled to a V_{DD} signal and a source of the second transistor is coupled to a V_{SS} signal.

23. An integrated circuit device receiving signals from a signal pad, comprising:
a first plurality of serially coupled substrate-biased silicon diodes responsive to the signals from the signal pad for providing electrostatic discharge protection from the signals, each of the first plurality of substrate-biased silicon diodes including a p-portion and an n-portion;

a second plurality of serially coupled substrate-biased silicon diodes responsive to the signals from the signal pad for providing electrostatic discharge protection from the signals, each of the second plurality of substrate-biased silicon diodes including a p-portion and an n-portion; and

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a detection circuit for detecting signals from the signal pad and providing a bias voltage to the first and second plurality of substrate-biased silicon diodes,

wherein the signal pad is coupled to the p-portion of one of the first plurality of substrate-biased silicon diodes and the n-portion of one of the second plurality of the substrate-biased silicon diodes.

24. The integrated circuit device as claimed in claim 23, wherein the detection circuit comprises a first transistor, a second transistor, and a resistor-capacitor network, and wherein a gate of the first transistor is coupled to a gate of the second transistor and the resistor-capacitor circuit.

25. The integrated circuit device as claimed in claim 24, wherein a drain of the first transistor and a drain of the second transistor are coupled to a substrate of the first and second plurality of substrate-biased silicon diodes to provide a bias voltage to the first and second plurality of substrate-biased silicon diodes.

26. An integrated circuit device, comprising

- a semiconductor substrate;
- an insulator layer disposed over the semiconductor substrate;
- a silicon layer disposed over the insulator layer, including
- a first isolation structure formed inside the silicon layer, and

a second isolation structure formed inside the silicon layer and spaced apart from the first isolation structure;

a dielectric layer disposed over the silicon layer; and

a layer of silicon, disposed over the dielectric layer, including a p-type portion, an n-type portion and a center portion disposed between and contiguous with the p-type and n-type portions.

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27. The integrated circuit device as claimed in claim 26, wherein the center portion of the layer of silicon overlaps a portion of the silicon layer between the first and second isolation structures.

28. The integrated circuit device as claimed in claim 26, wherein the portion of the silicon layer between the first and second isolation structures is biased to provide electrostatic discharge protection.

29. A silicon-on-insulator circuit device receiving signals from a signal pad, comprising at least one base-biased silicon diode, responsive to the signals from the signal pad, for providing electrostatic discharge protection.

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30. The silicon-on-insulator circuit device as claimed in claim 29, wherein each of the at least one base-biased silicon diodes includes a p-type polysilicon portion, an n-type polysilicon portion and a center polysilicon portion disposed between and contiguous with the p-type and n-type polysilicon portions.

31. The silicon-on-insulator circuit device as claimed in claim 29, wherein the silicon-on-insulator circuit device is biased to control the at least one base-biased silicon diode.

32. An integrated circuit device receiving signals from a signal pad, comprising one or more serially coupled base-biased silicon diodes, responsive to the signals from the signal pad, for providing electrostatic discharge protection.

33. The integrated circuit device as claimed in claim 32, further comprising a detection circuit for detecting signals from the signal pad and providing a bias voltage to the one or more base-biased silicon diodes, wherein the detection circuit comprises a resistor-capacitor network coupled in parallel to a transistor network.

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34. The integrated circuit device as claimed in claim 33, wherein the transistor network includes a first transistor and a second transistor, and wherein a gate of the first transistor is coupled to a gate of the second transistor and the resistor-capacitor network, and wherein a drain of the first transistor and a drain of the second transistor are coupled to a base of the one or more base-biased silicon diodes to provide a bias voltage.

35. A method for protecting a silicon-on-insulator device from electrostatic discharge, comprising the steps of:

providing a signal to the device through a silicon-on-insulator circuit;

providing a base-biased silicon diode in the silicon-on-insulator circuit; and

protecting the device from electrostatic discharge with the base-biased silicon diode.

36. A method for protecting a complementary metal-oxide semiconductor device from electrostatic discharge, comprising the steps of:

providing a signal to the device through a complementary metal-oxide semiconductor circuit;

providing a substrate-biased silicon diode in the complementary metal-oxide semiconductor circuit; and

protecting the device from electrostatic discharge produced from the signal with the substrate-biased silicon diode.

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37. A method for forming a silicon diode, comprising the steps of:

forming a first silicon layer;

forming a first isolation structure and a second isolation structure inside the first silicon layer, the first isolation structure being spaced apart from the second isolation structure;

forming a dielectric layer over the silicon layer;

forming a second silicon layer over the dielectric layer;

forming dielectric spacers contiguous with the second silicon layer;

implanting a first impurity having a first concentration into a first portion and a second portion of the second silicon layer, the first portion being contiguous with the second portion and the second portion overlapping a region of the first silicon layer between the first isolation structure and the second isolation structure;

implanting a first impurity having a second concentration into the first portion of the second silicon layer, wherein the second concentration is greater than the first concentration; and

implanting a second impurity into a third portion of the second silicon layer, wherein the third portion is contiguous with the second portion.

38. The method as claimed in claim 37, wherein the silicon layer is a semiconductor substrate.

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39. The method as claimed in claim 37, further comprising a step of forming a well region inside the semiconductor substrate, wherein the first and second isolation structures are disposed inside the well region.

40. The method as claimed in claim 37, wherein the first impurity is an n-type impurity and the second impurity is a p-type impurity.

41. The method as claimed in claim 37, wherein the first impurity is a p-type impurity and the second impurity is an n-type impurity.

42. The method as claimed in claim 37, wherein the step of forming a first and second isolation structures comprises the steps of forming a first trench and a second trench spaced apart from the first trench in the silicon layer, and providing a dielectric material in the first and second trenches.

43. The method as claimed in claim 37, wherein the step of forming a dielectric layer includes a step of growing an oxide layer.

44. The method as claimed in claim 37, wherein the steps of implanting a first impurity having a first concentration and implanting a first impurity having a second concentration create a diffused region adjacent one of first and second field isolation structures.

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45. The method as claimed in claim 37, wherein the step of implanting a first impurity having a first concentration includes the steps of

providing a photoresist over the first silicon layer and the second silicon layer;

patterning and defining the photoresist to expose the first portion and the

5 second portion of the second silicon layer,

implanting the first impurity into the first portion and the second portion, and

removing the photoresist.

46. The method as claimed in claim 37, wherein the step of implanting a second impurity includes the steps of

providing a photoresist over the second silicon layer and the silicon layer,

patterning and defining the photoresist to expose the third portion of the

5 second silicon layer,

implanting the second impurity into the third portion, and

removing the photoresist.

47. The method as claimed in claim 37, further comprising:

defining a substrate;

forming a layer of insulator over the substrate; and

forming the layer of silicon over the insulator layer.

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48. A method for forming a base-biased silicon diode, comprising the steps of:

forming a first and second isolation structures inside a silicon layer;

defining a base region inside the silicon layer, the base region being disposed between and contiguous with the first and second isolation structures;

5 forming a dielectric layer over the well region;

forming a layer of silicon over the dielectric layer;

implanting a first impurity having a first concentration into a first portion and a second portion of the silicon layer, wherein the first portion is contiguous with the second portion and the second portion overlapping a region of the silicon layer

10 between the first isolation structure and the second isolation structure;

implanting a first impurity having a second concentration into the first portion and second portion of the silicon layer, wherein the second concentration is greater than the first concentration; and

15 implanting a second impurity into a third portion of the silicon layer, wherein the third portion is contiguous with the second portion and overlaps the second isolation structure.

49. The method as claimed in claim 48, wherein the silicon layer is a silicon layer of a silicon-on-insulator structure.

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50. A method for forming a substrate-biased silicon diode, comprising the steps of:

forming a first isolation structure and a second isolation structure spaced apart from the first isolation structure inside a silicon layer;

forming a dielectric layer over the silicon layer;

forming a layer of silicon having two ends over the dielectric layer;

forming dielectric spacers contiguous with the two ends of the silicon layer;

implanting a first impurity having a first concentration into a first portion and a second portion of the silicon layer, wherein the first portion is contiguous with the second portion and overlaps the first isolation structure;

implanting a second impurity into a third portion of the silicon layer, wherein the third portion is contiguous with the second portion and overlaps the second isolation structure; and

implanting a first impurity having a second concentration into the first portion of the silicon layer, wherein the second concentration is greater than the first concentration.

51. The method as claimed in claim 50, wherein the step of implanting a second impurity creates a diffused region adjacent one of first and second field isolation structures.

52. An integrated circuit device used for electrostatic discharge protection,
comprising:

a semiconductor substrate;

a dielectric layer disposed over the substrate; and

5 a layer of silicon, formed over the dielectric layer, including a p-type portion
and an n-type portion.

53. An integrated circuit device used for electrostatic discharge protection,
comprising:

a semiconductor substrate;

a dielectric layer disposed over the substrate;

5 a layer of silicon, formed over the dielectric layer, including a p-type portion,
an n-type portion, and a center portion disposed between the n-type and p-type
portions.

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